<u>WHAT IS CLAIMED IS</u>:

1. A method, comprising:

receiving a multicast packet to transmit to destination addresses;

writing a payload of the multicast packet to at least one packet entry in a packet memory;

generating headers for the destination addresses;

generating at least one descriptor addressing the at least one packet entry in the packet memory including the payload to transmit to the destination addresses; and

generating, for each destination address, at least one indicator including information on the generated header for the destination address and the at least one descriptor, wherein indicators for the destination addresses address the at least one descriptor.

2. The method of claim 1, wherein the payload is written to multiple packet entries in the packet memory, wherein one descriptor is generated for each packet entry including the payload, and wherein one indicator is generated for each descriptor and destination address to which the payload in the packet entry addressed by the descriptor is transmitted.

3. The method of claim 2, further comprising:

for each destination address, setting a next handle in the indicators for the destination address to point to the indicator corresponding to the descriptor addressing a next entry in the packet memory including further payload data for the destination address.

4. The method of claim 1, wherein the payload is written to one packet entry in the packet memory, wherein one descriptor is generated for the packet entry including the payload, and wherein one indicator is generated for each destination address to which the payload in the packet entry addressed by the descriptor is transmitted.

5. The method of claim 1, further comprising:

generating a handle for each generated indicator addressing the indicator in a queue.

6. The method of claim 1, further comprising:

using, for each destination address and indicator associated with the destination address, the information on the generated header in the at least one indicator for the destination address to access the header for the destination address; and

transmitting, for each destination address and indicator associated with the destination address, the payload from the entry in the packet memory associated with the indicator and the accessed header for the destination address.

7. The method of claim 6, further comprising:

using, for each destination address, the header length and offset from the at least one indicator for the destination address to access the header for the destination address from the at least one entry in the packet memory addressed by the at least one descriptor identified in the at least one indicator for the destination address; and

transmitting, for each destination address, the payload from the entry in the packet memory and the accessed header for the destination address.

8. The method of claim 1, further comprising:

writing the generated headers to each entry in the packet memory including packet payload, wherein the information on the header in one indicator for one destination address includes a header length and offset used to extract the header from the entry in the packet memory for the destination address for which the indicator is generated.

9. The method of claim 8, wherein the indicator further includes information on a payload length and payload offset used to extract the payload from the entry for the destination address for which the indicator is generated, further comprising:

using, for each destination address, the payload length and offset information in the at leas tone indicator for the destination address to access the payload from the

at least one entry in the packet memory addressed by the at least one descriptor identified in the at least one indicator for the destination address.

10. The method of claim 1, further comprising:

writing to a local memory at least one handle for each destination address addressing the at least one indicator for the destination address; and

writing the handles in the local memory to an output queue; and

queuing the indicators corresponding to the handles in the output queue to at least one packet queue.

11. The method of claim 10, further comprising:

writing to the local memory information on one output queue for the handle written to the memory indicating the output queue to which the destination packet generated from the indicator addressed by the handle is queued.

12. The method of claim 10, wherein a packet processing block performs the operations of writing the payload, generating the headers, generating the at least one descriptor, generating the at least one indicator, writing the handles to the local memory, and writing the handles to the output queue, and where a transmission block uses the handles to access the indicators for the destination address to send the payload to the destination addresses.

13. A system, comprising:

a packet memory; and

circuitry in communication with the packet memory and enabled to:

(i) receive a multicast packet to transmit to destination addresses;

(ii) write a payload of the multicast packet to at least one packet entry in the packet memory;

(iii) generate headers for the destination addresses;

(iv) generate at least one descriptor addressing the at least one packet entry in the packet memory including the payload to transmit to the destination addresses; and

(v) generate, for each destination address, at least one indicator including information on the generated header for the destination address and

the at least one descriptor, wherein indicators for the destination addresses address the at least one descriptor.

14. The system of claim 13, wherein the payload is written to multiple packet entries in the packet memory, wherein one descriptor is generated for each packet entry including the payload, and wherein one indicator is generated for each descriptor and destination address to which the payload in the packet entry addressed by the descriptor is transmitted.

15. The system of claim 14, wherein the circuitry is enabled to:

for each destination address, set a next handle in the indicators for the destination address to point to the indicator corresponding to the descriptor addressing a next entry in the packet memory including further payload data for the destination address.

16. The system of claim 13, wherein the payload is written to one packet entry in the packet memory, wherein one descriptor is generated for the packet entry including the payload, and wherein one indicator is generated for each destination address to which the payload in the packet entry addressed by the descriptor is transmitted.

17. The system of claim 13, wherein the circuitry is further enabled to:

generate a handle for each generated indicator addressing the indicator in a queue.

18. The system of claim 13, wherein the circuitry is further enabled to:

use, for each destination address and indicator associated with the destination address, the information on the generated header in the at least one indicator for the destination address to access the header for the destination address; and

transmit, for each destination address and indicator associated with the destination address, the payload from the entry in the packet memory associated with the indicator and the accessed header for the destination address.

19. The system of claim 18, wherein the circuitry is further enabled to:

use, for each destination address, the header length and offset from the at least one indicator for the destination address to access the header for the destination address from the at least one entry in the packet memory addressed by the at least one descriptor identified in the at least one indicator for the destination address; and

transmit, for each destination address, the payload from the entry in the packet memory and the accessed header for the destination address.

20. The system of claim 13, wherein the circuitry is further enabled to:

write the generated headers to each entry in the packet memory including packet payload, wherein the information on the header in one indicator for one destination address includes a header length and offset used to extract the header from the entry in the packet memory for the destination address for which the indicator is generated.

21. The system of claim 20,wherein the indicator further includes information on a payload length and payload offset used to extract the payload from the entry for the destination address for which the indicator is generated, wherein the circuitry is further enabled to:

use, for each destination address, the payload length and offset information in the at leas tone indicator for the destination address to access the payload from the at least one entry in the packet memory addressed by the at least one descriptor identified in the at least one indicator for the destination address.

22. The system of claim 13, further comprising:

a local memory;

wherein the circuitry is further enabled to:

(i) write to the local memory at least one handle for each destination address addressing the at least one indicator for the destination address; and

(ii) write the handles in the local memory to an output queue; and

(iii) queue the indicators corresponding to the handles in the output queue to at least one packet queue.

23. The system of claim 22, wherein the circuitry is further enabled to:

write to the local memory information on one output queue for the handle written to the memory indicating the output queue to which the destination packet generated from the indicator addressed by the handle is queued.

24. The system of claim 22, wherein a packet processing block performs the operations of writing the payload, generating the headers, generating the at least one descriptor, generating the at least one indicator, writing the handles to the local memory, and writing the handles to the output queue, and where a transmission block uses the handles to access the indicators for the destination address to send the payload to the destination addresses.

25. The system of claim 24, wherein the circuitry comprises a plurality of packet engines, wherein one packet engine executes the packet processing block and another packet engine executes the transmission block.

26. A system, comprising:

a switch fabric; and

a plurality of line cards coupled to the switch fabric, wherein each line card includes a network processor, wherein each network processor includes:

(i) a packet memory; and

(ii) circuitry in communication with the packet memory and enabled to:

(a) receive a multicast packet to transmit to destination addresses;

(b) write a payload of the multicast packet to at least one packet entry in the packet memory;

(c) generate headers for the destination addresses;

(d) generate at least one descriptor addressing the at least one packet entry in the packet memory including the payload to transmit to the destination addresses; and

(e) generate, for each destination address, at least one indicator including information on the generated header for the destination address and the at least one descriptor, wherein indicators for the destination addresses address the at least one descriptor.

27. The system of claim 26, wherein the payload is written to multiple packet entries in the packet memory, wherein one descriptor is generated for each packet entry including the payload, and wherein one indicator is generated for each descriptor and destination address to which the payload in the packet entry addressed by the descriptor is transmitted.

28. The system of claim 26, wherein the circuitry is further enabled to:

write the generated headers to each entry in the packet memory including packet payload, wherein the information on the header in one indicator for one destination address includes a header length and offset used to extract the header from the entry in the packet memory for the destination address for which the indicator is generated.

29. An article of manufacture for transmitting packets, wherein the article of manufacture is in communication with a packet memory and causes operations to be performed, the operations comprising:

receiving a multicast packet to transmit to destination addresses;

writing a payload of the multicast packet to at least one packet entry in a packet memory;

generating headers for the destination addresses;

generating at least one descriptor addressing the at least one packet entry in the packet memory including the payload to transmit to the destination addresses; and

generating, for each destination address, at least one indicator including information on the generated header for the destination address and the at least one descriptor, wherein indicators for the destination addresses address the at least one descriptor.

30. The article of manufacture of claim 29, wherein the payload is written to multiple packet entries in the packet memory, wherein one descriptor is generated for each packet entry including the payload, and wherein one indicator is generated for each descriptor and destination address to which the payload in the packet entry addressed by the descriptor is transmitted.

31. The article of manufacture of claim ~~32~~ 30, wherein the operations further comprise:

for each destination address, setting a next handle in the indicators for the destination address to point to the indicator corresponding to the descriptor addressing a next entry in the packet memory including further payload data for the destination address.

32. The article of manufacture of claim 29, wherein the payload is written to one packet entry in the packet memory, wherein one descriptor is generated for the packet entry including the payload, and wherein one indicator is generated for each destination address to which the payload in the packet entry addressed by the descriptor is transmitted.

33. The article of manufacture of claim 29, wherein the operations further comprise:

generating a handle for each generated indicator addressing the indicator in a queue.

34. The article of manufacture of claim 29, wherein the operations further comprise:

using, for each destination address and indicator associated with the destination address, the information on the generated header in the at least one indicator for the destination address to access the header for the destination address; and

transmitting, for each destination address and indicator associated with the destination address, the payload from the entry in the packet memory associated with the indicator and the accessed header for the destination address.

35. The article of manufacture of claim 34, wherein the operations further comprise:

using, for each destination address, the header length and offset from the at least one indicator for the destination address to access the header for the destination address from the at least one entry in the packet memory addressed by the at least one descriptor identified in the at least one indicator for the destination address; and

transmitting, for each destination address, the payload from the entry in the packet memory and the accessed header for the destination address.

36. The article of manufacture of claim 29, wherein the operations further comprise:

writing the generated headers to each entry in the packet memory including packet payload, wherein the information on the header in one indicator for one destination address includes a header length and offset used to extract the header from the entry in the packet memory for the destination address for which the indicator is generated.

37. The article of manufacture of claim 36, wherein the indicator further includes information on a payload length and payload offset used to extract the payload from the entry for the destination address for which the indicator is generated, further comprising:

using, for each destination address, the payload length and offset information in the at leas tone indicator for the destination address to access the payload from the at least one entry in the packet memory addressed by the at least one descriptor identified in the at least one indicator for the destination address.

38. The article of manufacture of claim 29, wherein the article of manufacture is further coupled to a local memory, wherein the operations further comprise:

writing to the local memory at least one handle for each destination address addressing the at least one indicator for the destination address; and

writing the handles in the local memory to an output queue; and

queuing the indicators corresponding to the handles in the output queue to at least one packet queue.

39. The article of manufacture of claim 38, further comprising:

writing to the local memory information on one output queue for the handle written to the memory indicating the output queue to which the destination packet generated from the indicator addressed by the handle is queued.

40. The article of manufacture of claim 38, wherein a packet processing block performs the operations of writing the payload, generating the headers, generating the at least one descriptor, generating the at least one indicator, writing the handles to the local memory, and writing the handles to the output queue, and where a transmission block uses the handles to access the indicators for the destination address to send the payload to the destination addresses.